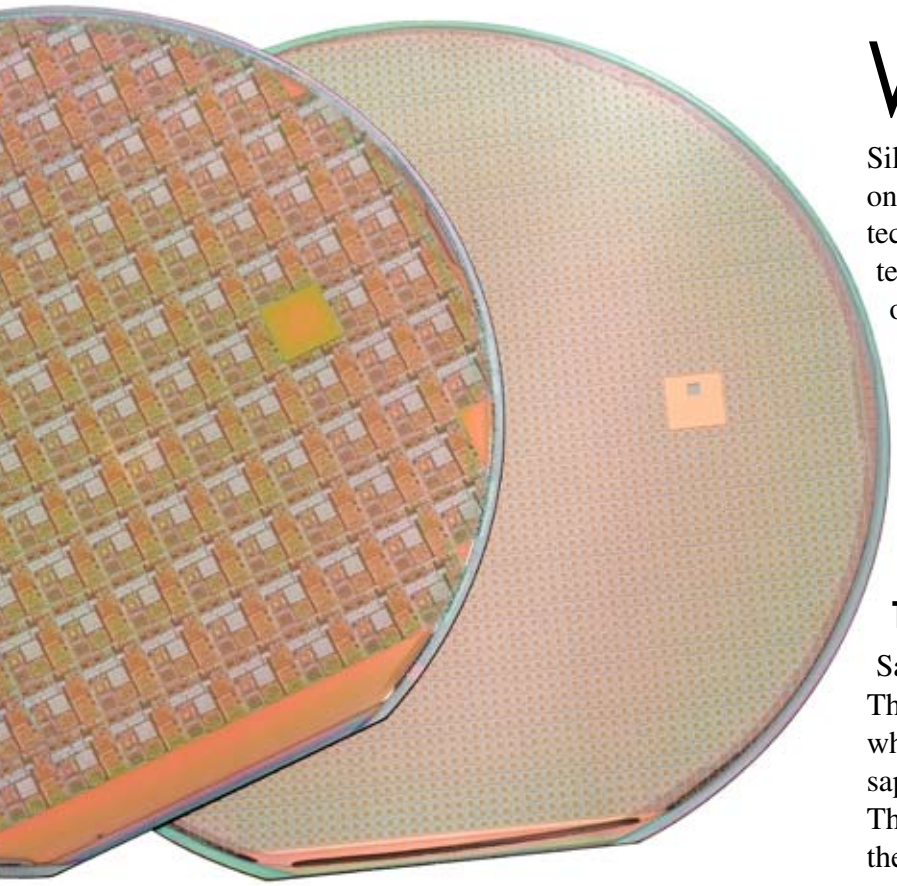

"This is again one of those developments where with very little trouble you can talk yourself completely out of even trying the experiment. No crystallographer would try the experiment because the match is just not good enough that you could hope that the silicon atoms would come down and sit in the right spots so that later ones would again come down and make a single crystal."[1]

– Charles Mueller of RCA Laboratories, on depositing silicon on sapphire.

The History of Silicon-on-Sapphire

by George Imthurn, Device Engineer
Peregrine Semiconductor Corporation

What is Silicon-on-Sapphire?

Silicon-on-Sapphire (SOS) is one of the silicon-on-insulator (SOI) semiconductor manufacturing technologies. In fact, SOS is the first of the SOI technologies. SOS is formed by depositing a thin layer of silicon onto a sapphire wafer at high temperature. Its main advantage for electronic circuits is the highly insulating sapphire substrate. The benefit of the insulating substrate is very low parasitic capacitance, which provides increased speed, lower power consumption, better linearity, and more isolation than bulk silicon.

The Sapphire Wafer

Sapphire is also known as corundum or α-alumina. This sapphire is the same crystal that is called a ruby when it contains chromium as an impurity, or blue sapphire when the impurities are iron and titanium. The sapphire wafers used in SOS are not dug from the ground, as gemstones are, but grown as a large crystal in a controlled environment. The result is an extremely pure single crystal of sapphire that can weigh more than 50 kg. The sapphire wafer is not cut on the crystal axis of symmetry, but instead is cut at an angle of about 60° along what is called the "r-plane". In crystallographic notation this is the $(1\bar{1}02)$ plane.

How can the completely dissimilar silicon crystal be grown on sapphire? In a remarkable phenomenon of nature, the r-plane of sapphire has oxygen atoms spaced at a distance that is close to the spacing of the atoms in the (100) plane of a silicon crystal. The oxygen atoms on the r-plane have a square symmetry that also mirrors the symmetry of the (100) plane of silicon. The (100) plane of silicon is the same crystal plane that is used in all CMOS electronics. The square symmetry of the r-plane of sapphire is illustrated in Figure 1. Notice that there is an extra oxygen atom available in each set of four. A silicon atom can bond to one of the corner oxygen atoms in addition to this one to form a simple SiO2 bond. The extra oxygen atom is spaced at approximately the distance between the oxygen atoms in single crystal SiO2. The remarkable compatibility between the $(1\bar{1}02)$ plane of sapphire and the (100) plane of silicon is what enables SOS technology.

The History of Silicon-on-Sapphire

SOS was invented in 1963 at North American Aviation (now Boeing), Autonetics Division in Anaheim, California. The first published report is by Harold Manasevit and William Simpson [2]. A very practical experiment led to the discovery of SOS. A sapphire crystal was polished into a spherical shape and immersed in a gas containing silicon. A spherical surface will expose all of the planes that exist in a crystal system. It was found that (100) silicon grew in certain sites on the sphere, and these were identified as corresponding to the $(1\bar{1}02)$ plane of sapphire. Manasevit also deposited silicon films on spinel and cubic zirconia, but these technologies never made it out of the laboratory.

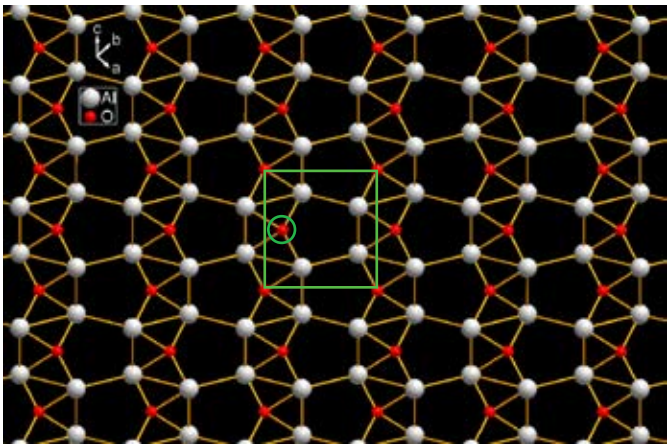

Figure 1. A view of the r-plane of sapphire. The green box illustrates the square symmetry of the oxygen atoms. The green circle shows the extra oxygen atom that is used in the SiO2 bond. The yellow rods represent atomic bonds.

In the mid-1960s researchers at the RCA Laboratories in Princeton, New Jersey worked on making SOS a manufacturable technology. The primary application was for radiation hard circuits, but these researchers also realized the speed and low power benefits of SOS could lead to commercial applications. RCA led the development of SOS technology into the mid-1970s and in fact still processes SOS for space applications.

The first attempt at commercializing SOS was by a company named Inselek, a spin-off of RCA. The early 1970s were a time where the future seemed bright for SOS. In a review article in 1972, Edward Ross of Inselek wrote that, "The principal metallurgical, chemical and electrical properties of SOS films prove to be as good as, or better than, those of chemically or mechanically polished bulk silicon wafers" [3]. Inselek did not survive into the 1980s.

The one notable commercial application of SOS in the late 1970s and into the 1980s was in the Hewlett-Packard 41-Series calculators. SOS was adopted by Hewlett-Packard because of its low power consumption. Soon bulk silicon captured the low power market and has only recently been displaced by SOI.

The technological barrier to SOS becoming commercially successful in the 1970s was the high number of defects in the film. The defects cause leakage current when the transistor is off and reduce carrier mobility. Mobility is a measurement of how fast charge can accelerate in a semiconductor, or indirectly, a transistor's maximum frequency of operation. It had been known for some years that as the silicon film is grown thicker, the quality of the film improves and the mobility increases. High resolution images of the atomic structure, such as is shown in Figure 2, show how the defects grow together and cancel each other, leading to a higher quality film farther away from the silicon/sapphire interface.

SOS was successfully used in these thicker films where the defect density is reduced, but in order to achieve really high performance, an ultra-thin film is required. An ultra-thin film is generally considered to be less than 100 nm, or only about 100 atoms, thick. Ultra-thin films enable the use of shorter gate lengths, which of course leads to higher speed electronics.

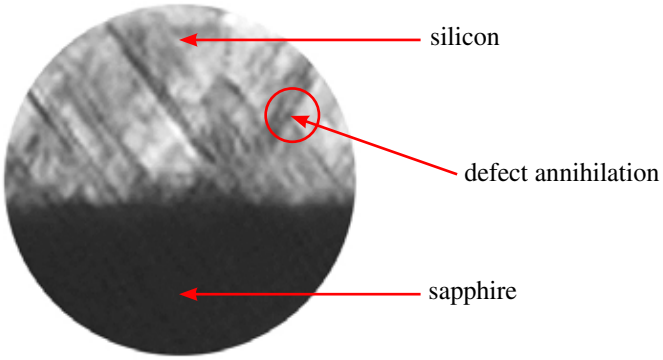

Figure 2. The red circle highlights the defect annihilation in the SOS film as the film thickness increases.

Ultra-Thin Silicon Film

Another advantage of ultra-thin films is that so-called "fully-depleted" transistors may be used. Without going into detailed semiconductor physics, "fully-depleted" simply means that the conducting channel of the transistor is depleted of charge by the time the transistor turns on. This can only occur in SOI

technologies because in bulk silicon there is an almost infinite source of charge available that can not be depleted. The performance advantage of fully-depleted transistors comes from the fact that when there is no charge in the channel, the entire gate voltage is applied to create a conducting channel. This essentially acts like a thinner gate oxide, increasing the drive current of the transistor.

The breakthrough that enabled ultra-thin SOS films was developed by Silvanus Lau at the California Institute of Technology and researchers at Hewlett-Packard in 1978 [4]. The process is called Solid Phase Epitaxial Regrowth (SPER). The first part of SPER is a silicon implant. The implant parameters are set so that the silicon crystal is amorphized in the region near the sapphire interface, but the better quality crystal away from the interface is left intact. An anneal then regrows the amorphous silicon into a single crystal by using the upper layer of the film as a template. The final step is the thinning of the silicon layer to about 100 nm thickness by oxidation. Figure 3 provides a schematic illustration of the SPER process.

A. "As-grown" SOS with twinning defects shown in red. These defects cancel each other when they merge higher up in the silicon layer.

B. SOS after the silicon amorphization implant. The region near the silicon/ sapphire interface no longer has any crystal structure.

C. "Improved" SOS, where the crystal has been regrown from the crystal lattice template at the upper surface of the silicon layer.

Figure 3. A schematic representation of the Solid Phase Epitaxial Regrowth (SPER) process.

The SPER technique was never used commercially by Hewlett-Packard. Work continued on refining this process, however, at the Naval Ocean Systems Center (NOSC) in San Diego, California. It was at NOSC that the RF applications of ultra-thin SOS began to be explored. In 1990, former NOSC researchers Dr. Ron Reedy and Dr. Mark Burgener, along with partner Rory Moore, founded Peregrine Semiconductor in San Diego, California. Their purpose was to commercialize ultra-thin SOS. Significant patent work ensued and during the next few years, Peregrine Semiconductor began to market space-level Ultra-Thin Silicon-on-Sapphire (UTSi®) devices. Though there are still other manufacturers of SOS, Peregrine is the only company that has achieved a commercially viable product portfolio, consisting of RF switches, digital step attenuators, phase locked-loop synthesizers, mixers and pre-scalers, working at frequencies up to 12GHz. While this once-specialized and expensive military technology is now found in a variety of RF communications electronics, it is still used in many space applications, for which it was originally intended.

Why SOS?

Though SOS is not a new technology, it has only recently won broad acceptance in high-volume commercial applications. Before the advent of ultra-thin SOS films this was largely due to technological barriers. By the mid 1980s, when the performance of SOS was proven, bulk silicon technology was progressing so quickly that the barriers to the commercial success of SOS became economic. What has enabled the commercial success of SOS in the 21st century is the ubiquity of wireless communications. Wireless RF applications do not require very high density circuitry as a microprocessor does, nor do they require functional frequencies of tens of GHz. Wireless applications benefit from operation at a few GHz and moderate amounts of digital integration that consume very little power.

Why has SOS found its niche in wireless communication? The answer lies in its relation to the dominant semiconductor technology…CMOS on bulk silicon. SOS benefits both from its differences and similarities to bulk silicon. Recognizing the potential impact on the design and development of a wide variety of RF applications, Peregrine Semiconductor began to market its proprietary high-performance SOS process, UltraCMOS™ technology.

UltraCMOS - changing the way RF is designed

The most important advantage of UltraCMOS over bulk silicon technology is its insulating substrate. The insulating substrate virtually eliminates the parasitic drain capacitance that is present in bulk silicon. This does several important things. The simple thing is that it leads to dramatic improvement in transistor performance because this capacitor does not need to be charged and discharged on every cycle. The insulating substrate also provides better isolation between circuit elements. More subtly, because the drain capacitor in bulk silicon is a depletion capacitance between two semiconductor layers it behaves in a non-linear manner. Eliminating this non-linearity enables UltraCMOS to have significantly better harmonic performance than bulk silicon. In fact, one of the most important performance advantages of III-V semiconductor compounds is their semi-insulating substrates.

The farthest man-made object from the earth, the Voyager 1 spacecraft, has an RCA-built SOS microprocessor aboard it. It was launched in 1977 and left our solar system in 2003. As of January 2006 it was 14 billion kilometers from earth and still functioning.

UltraCMOS benefits from its similarity to bulk silicon by its use of the same basic CMOS technology. The reason that bulk silicon dominates the semiconductor market is not because of raw performance. Certainly, exotic III-V semiconductor technologies (such as GaAs) have better electron mobility and higher breakdown fields than silicon. The key to bulk silicon's success is in the fundamental benefits of standard CMOS processing; that is: high manufacturing yields, low power operation and high levels of integration. UltraCMOS benefits from all the process refinements that have been developed for CMOS on bulk silicon, and from the existing manufacturing infrastructure that was assembled around silicon.

But the best performing technology will not always win in the marketplace. Commercial success requires economic advantages also. A big advantage of UltraCMOS over exotic technologies is that it is manufactured in the same factories that produce common bulk silicon wafers. A further advantage is that, because of its better performance, it can be manufactured in a less advanced factory than similar devices in bulk silicon. The performance that is obtained for a given technology in UltraCMOS is about two generations ahead of the performance of bulk silicon. For example, the 0.25µm technology node in SOS has similar performance to the 0.13µm node in bulk silicon. The cost savings from utilizing 'lagging-edge' semiconductor technology rather than leading-edge technology are enormous. These savings show up not only in the much higher equipment and depreciation costs associated with later generation process technology, but also in the dramatically higher wafer mask costs associated with the smaller geometry processes. And though SOS wafers are, and probably always will be, more expensive than bulk silicon wafers, they are less expensive than substrates used for III-V technologies providing similar performance.

Modern wireless systems are at the confluence where having the integration capabilities and infrastructure of CMOS along with the performance of III-V materials make SOS an extremely viable commercial technology. Today, Peregrine works with the most highly respected and visionary wireless communications system manufacturers in the world to remove RFIC performance roadblocks and develop UltraCMOS-based design solutions for tomorrow's highly integrated products.

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About the Author

George Imthurn is a Device Engineer for Peregrine Semiconductor Corporation, a manufacturer of UltraCMOS-based RFICs. During his tenure at Peregrine he has contributed to the basic understanding of SOS and worked on improving the radiation hardness of the UltraCMOS process. Before joining Peregrine he worked on SOS at the Naval Ocean Systems Center. George received his BS at Pacific Union College and his MSEE at San Diego State University. His thesis work was on guided wave optics.